UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,879,195 B2
DATED : April 12, 2005
INVENTOR(S) : Michael Green et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 10,
Lines 27-39, claim 20 should read:
A circuit comprising:
a phase-locked loop circuit that receives a reference clock signal and generates a feedback clock signal; and
means for detecting when the feedback clock signal and the reference clock signal are out of lock, wherein the means detects that the feedback clock signal and the reference clock signal are out of lock when a like number of feedback clock cycles and reference clock cycles occur during a time period and when a single rising edge and a single falling edge of the feedback clock signal are detected during less than a predetermined number of the reference clock cycles during the time period.

Signed and Sealed this

Second Day of August, 2005

JON W. DUDAS
Director of the United States Patent and Trademark Office